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Impact of Power-Performance of MAC Units in VLSI Technologies

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ABSTRACT

The impact of power–performance trade-offs of Multiply–Accumulate (MAC) units in VLSI technologies is significant in determining the overall efficiency of modern digital systems. MAC units are core components in digital signal processing (DSP), artificial intelligence (AI), multimedia processing, and communication systems, where high-speed computation is essential. In VLSI design, improving performance typically involves increasing clock frequency, parallelism, and pipeline depth; however, these enhancements often lead to higher dynamic and leakage power consumption. As technology scales into deep submicron regions, leakage currents and short-channel effects further intensify power challenges, making efficient power-performance optimization critical. A well-balanced power–performance design ensures high throughput while maintaining minimal energy dissipation. Techniques such as voltage scaling, clock gating, operand isolation, and optimized multiplier architectures (e.g., Booth encoding and Wallace tree structures) help achieve this balance. Lowering supply voltage significantly reduces dynamic power but may impact speed, requiring careful architectural and circuit-level optimization. The adoption of advanced fabrication technologies such as FinFET and multi-gate devices also enhances performance per watt. Additionally, approximate computing methods are increasingly applied in error-tolerant applications like image and speech processing to reduce power consumption with acceptable accuracy loss.