National Conference on Innovative Research in Science, Engineering and Technology (NCIRSET – 2019)
28TH July 2019, Hyderabad, Telangana, India

CERTIFICATE NO : NCIRSET /2019/ C0719523

# A STUDY OF NON-CONVENTIONAL METHODS OF LOW POWER DESIGN FOR ADIABATIC SWITCHING

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## ABSTRACT

The recent trends in the developments and advancements in the area of low power VLSI Design are surveyed in this paper. Though Low Power is a well-established domain, it has undergone lot of developments from transistor sizing, process shrinkage, voltage scaling, clock gating, etc., to adiabatic logic. This paper aims to elaborate on the recent trends in the low power design. Adiabatic logic works with the concept of switching activities which reduces the power by giving stored energy back to the supply. Thus, the term adiabatic logic is used in low-power VLSI circuits which implements reversible logic. In this, the main design changes are focused in power clock which plays the vital role in the principle of operation. Each phase of the power clock gives user to achieve the two major design rules for the adiabatic circuit design. During the recovery phase energy will be restored to the power clock, resulting in considerable energy saving. These include only turning switches on when there is no potential difference across them, only turning switches off when no current is flowing through them, and using a power supply that is capable of recovering or recycling energy in the form of electric charge. To achieve this, in general, the power supplies of adiabatic logic circuits have used constant current charging (or an approximation thereto), in contrast to more traditional non-adiabatic systems that have generally used constant voltage charging from a fixed-voltage power supply. The power supplies of adiabatic logic circuits have also used circuit elements capable of storing energy. This is often done using inductors, which store the energy by converting it to magnetic flux. There are a number of synonyms that have been used by other authors to refer to adiabatic logic type systems, these include: “Charge recovery logic”, “Charge recycling logic”, “Clock-powered logic”, “Energy recovery logic” and “Energy recycling logic”.

***Keywords: Low Power Design, Transistor Sizing, Process Shrinkage, Voltage Scaling, Clock Gating.***