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IMPACT OF LDPC CODES WITH BCH CODES ON AN FPGA PLATFORM

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ABSTRACT

The combination of Low-Density Parity-Check (LDPC) codes with Bose-Chaudhuri-Hocquenghem (BCH) codes on an FPGA (Field-Programmable Gate Array) platform significantly enhances error correction capabilities in digital communication systems. LDPC codes are known for their strong error-correcting performance, particularly in scenarios with high noise levels, but they typically require complex decoding algorithms. BCH codes, on the other hand, offer simpler decoding processes with a guaranteed ability to correct a specific number of errors, making them a valuable complementary code. On an FPGA platform, integrating LDPC and BCH codes allows for a flexible and high-performance error correction solution. FPGAs are ideal for implementing such algorithms due to their reconfigurable nature, enabling the parallel processing of data and the optimization of decoding speed. By using BCH codes to pre-correct errors before applying LDPC decoding, the overall error correction process becomes more robust and efficient. This hybrid approach can lead to a significant reduction in decoding latency, making it suitable for real-time applications such as wireless communication, digital broadcasting, and data storage systems. Moreover, the use of FPGAs allows for custom tuning of the error correction pipeline to balance performance, power consumption, and resource usage, meeting the specific demands of various applications.